REMARKS

Claims 1-44 are pending in the present application. In the Office Action dated August 29, 2007, the Examiner rejected claims 1, 2, under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,982,485 to Holmberg et al. ("the Holmberg patent"), claims 6,7 under 35 U.S.C. 102(b) as being anticipated by, or, in the alternative, under 35 U.S.C. 103(a) as being obvious over the Holmberg patent. The Examiner has also rejected claims 3-5, 8-13 under 35 U.S.C. 103(a) as being obvious over the Holmberg patent in view of U.S. Patent No. 4,078,228 to Miyazaki ("the Miyazaki patent"), claims 14-18, 22-26, 30, 32-35, 39, 41, 42 and 44 under 35 U.S.C. 103(a) as being obvious over U.S. Patent Publication No. 20040193821 to Ruhovets et al. ("the Ruhovets patent") in view of the Miyazaki patent, U.S. Patent No. 6,064,706 to Driskill et al. ("the Driskill patent"), and admitted prior art, and claims 19-21, 27-29, 36-38 and 43 under U.S.C. 103(a) as being obvious over the Ruhovets patent in view of the Miyazaki patent, the Driskill patent, the admitted prior art, and further in view of U.S. Patent Publication No. 20040160206 to Komaki et al.

The embodiments of the disclosed application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Embodiments of the present application are directed to synchronizing communication links in a memory hub architecture of a memory system. In one embodiment, the memory hub architecture includes a system controller and a plurality of memory hubs coupled together in series and to the system controller by a pair of downstream and upstream high-speed links. The system controller applies memory commands to control and access data in the memory modules that each contain a respective memory hub. The memory hubs communicate over the high-speed links to control access to a plurality of memory devices in each of the memory modules. The system controller is also enabled to execute a synchronization mode of operation to synchronize each of the high speed links and enable transmission and reception ports of the hub architecture for normal memory operations, such as receiving and transmitting data during memory operations.

The synchronization mode of operation is executed by the controller in two stages of operation. During an initialization stage, the controller determines a desired phase shift of a received clock signal relative to a test data signal for establishing phase shift limitations used to capture data signals transmitted during memory operations. The test data signal is transmitted onto the downstream link from a transmission port of the controller to a reception port of the first memory module, and then to the next adjacent link in a clockwise manner until the test data signal is returned on an upstream link and received by a reception port of the controller. The transmission and reception ports of each memory hub receives the test data signal on respective links and adjusts the phase of the received clock signal relative to the test data signal. Once a final phase of the received clock signal is determined, the controller executes an inversion signal that is similarly transmitted in a clockwise manner to each of the links, and indicates to the receiving port that the previous port and link have been synchronized. When the reception port of the controller receives the inversion signal, the controller determines that all the links and corresponding ports have been synchronized, and provides an enablement command signal to initiate an enablement stage. In one embodiment, the enablement command signal is represented by a NOP signal. As each link receives the NOP signal, each of the links are enabled, and the system is placed in a normal mode of operation, the enablement stage being complete once the NOP signal returns to the reception port of the controller.

The Examiner has cited the Holmberg reference, which is directed to a computer network system that utilizes measurement devices for taking weight measurements, for example of an airplane, and to convert the measurements into digital signals. The computer network system includes a master node coupled to a plurality of slave nodes interconnected by communication links in a ring formation. In contrast to the embodiments of the present application, the master node does not synchronize the downstream and upstream links for processing functional memory commands. Instead, the master node initiates a synchronizing message to the slave nodes on the communication links so that each slave node, upon receiving the synchronizing message, can determine its own delay period for synchronizing with the other slave nodes. When the slave nodes have all been synchronized, by each slave node determining the proper delay relative to the other slave nodes, all the slave nodes begin measuring at the same time. In contrast, memory hubs in a memory system are synchronized to transfer and process

memory command operations across high-speed communication links, which is different from the manner in which the slave nodes are synchronized and the type of data that is transmitted as described by the Holmberg patent.

The Examiner has cited the Ruhovets patent for the purposes of disclosing a memory system having a plurality of memory modules coupled by point-to-point links to each other and to a memory controller. Each of the memory modules includes a memory buffer circuit for coupling the downstream and upstream links between the memory modules. The Ruhovets patent merely describes a conventional memory system that is well-known in the art, and does not provide any reason to modify its teachings so that each point-to-point link is synchronized before normal operations begin. In fact, the Ruhovets patent teaches a different means of clocking data on the links by relying on a clock signal generated by a phase-locked loop in the memory buffer circuit. The Examiner has also cited the admitted prior art in order to provide a purported teaching for modifying the disclosure of the Ruhovets patent, suggesting that the admitted prior art teaches operating the memory system in a synchronization mode. The admitted prior art, instead describes a need for a system and method of synchronizing memory hubs in a memory system. Since the Ruhovets patent merely discloses a conventional memory system, it does not add further teachings to the admitted prior art to suggest a functionality for a synchronization mode of operation.

The Examiner has also cited the Miyazaki patent to purportedly provide a teaching for an inversion signal after a final phase of a received clock signal is determined. The inversion signal described in the Miyazaki patent is instead generated responsive to a failed signal at a data station to block the signal from an interface to a highway transmission line in a data highway communication system. The Examiner also relies on the teachings of the Driskill patent that purportedly describes test data signals applied to an output and to adjust the value of the test data signals responsive to an inversion signal. The Driskill patent instead describes a digital desynchronizer that generates an output data signal responsive to an output clock signal. The clock rate of the output clock signal is controlled by jitter control signals to either speed up or slow down the clock signal, thereby increasing or decreasing the rate at which the output data signal is provided.

The combination of the teachings of the Ruhovets patent in view of the Miyazaki patent and the Driskill patent does not teach a memory system coupled to a controller that synchronizes the high-speed links and associated ports for function memory command operations. Instead, the combination of the teachings describe a very different system, and in fact, teaches away from the disclosed embodiments of the present application. The combination of the above references teaches a memory system that relies on a clock signal generated by a phase-locked loop to transmit data signals at varying transmission rates on a communication link. If such signals contain errors or fails, the signals may be blocked from transmission to the next memory hub. In such case, the controller will be unable to synchronize the memory hubs for direct communication since a final phase of a received clock signal cannot be determined if the clock speed is adjustable and since some of the data signals may be blocked from transmission. There is simply no teaching, either expressed or implied in the Ruhovets, Miyazaki and Driskill patents that teaches a system or method of synchronizing memory hubs in a memory system prior to normal memory operations.

Applicant understands that motivation to modify a reference does not need to be expressly articulated by the cited references, although if there is motivation to combine or modify a reference such motivation is usually expressly found in the references. However, the Examiner must still articulate a credible motivation to modify the cited references, either from express or implied teachings of the cited references or from knowledge commonly known to those of ordinary skill in the art. A reason has not been articulated why one of ordinary skill in the art would modify a conventional memory system as in the Ruhovets patent to include the step of synchronizing the memory hubs prior to normally operating the memory system. The Miyazaki and Driskill patents teach entirely different motivations to either block failed signals from propagating to the next reception port or to adjust the rate at which data signals are transmitted. Such modifications teach away from the disclosed embodiments of the present application.

Turning now to the claims, amended claim 1 is directed to a method of synchronizing communications links in a memory system by sequentially synchronizing downstream links and upstream links starting with the downstream link coupling the controller to a first memory module. The controller is indicated when the links have been synchronized so

that the controller may then sequentially enable all the downstream and upstream links to process functional memory commands. The Holmberg patent does not teach a method of synchronizing memory hubs for processing functional memory commands. Instead, the Holmberg patent describes synchronizing a plurality of slave nodes, by determining different delay times at each slave node relative to when a synchronization message was received, and to simultaneously conduct weight measurements and process the measurement data.

Amended claim 6 is directed to synchronizing upstream and downstream links in a memory hub system. The links are synchronized in a clockwise order to ensure that all the links have been properly synchronized so that a controller may sequentially enable the links, also in a clockwise order, to process functional memory commands. In contrast, the Holmberg patent does not describe synchronizing memory hubs in a memory hub system for processing functional memory commands. Instead, the Holmberg patent describes synchronizing a plurality of slave nodes by a master node to take weight measurements of objects, such as an airplane, and transmit the measurement data back to the master node for processing.

Amended claim 14 teaches a memory hub having a downstream reception interface and an upstream reception interface operable to adjust a phase of a generated receive clock signal relative to applied test data signals responsive to receiving an inversion signal. Each memory hub additionally includes a downstream transmission interface and an upstream transmission interface, each operable to apply test data signals on an output and adjust the value of the test data signals responsive to the inversion signal. Each of the interfaces are further operable to provide an enablement command on the output to place the memory hub into a normal mode of operation. Contrary to the amended claim 14, the combination of teachings by the Ruhovets patent in view of the Miyazaki and the Driskill patents does not describe adjusting the phase of a generated receive clock signal and adjusting the value of the test data signals responsive to the inversion signal during synchronization. Instead the combined teachings suggest a very different memory system that relies on a clock signal, generated by a phase-locked loop, to transmit data signals across communication links at varying rates and to block data signals from reception ports if the signals are failed signals.

Similarly, amended claims 22, 30 and 39 are directed to a memory module including the memory hub as described above, a memory system that includes a plurality of the

memory modules and a computer system that includes the memory system, respectively. For the same reasons stated above, the combined teachings of the Ruhovets, Miyazaki and Driskill patents do not disclose or fairly suggest including memory hubs capable of adjusting the phase of a generated receive clock signal and adjusting the value of the test data signals responsive to the inversion signal during a synchronization mode.

Claims depending from claims 1, 6, 14, 22, 30 and 39 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims. Additional claims 19, 20, 27, 28, 31, 36 and 40 are amended to obviate claim objections by the Examiner or to place the claim in better form. The amendments do not affect the scope of claims 19, 20, 27, 28, 31, 36 and 40.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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Enclosures:

- Postcard
- Fee Transmittal Sheet (+ copy)
- Supplemental Information Disclosure Statement
- Form PTO-1449
- 2 Sheets of Annotated Drawings (Figs 3 & 4)
- 4 Sheets of Replacement Drawings (Figs 1-4)

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